[Fig. 15-1] Fig. 15-1 represents a potential diagram corresponding to a certain timing of the timing chart shown in Fig. 14-1.

[Fig. 15-2] Fig. 15-2 represents a potential diagram corresponding to another certain timing of the timing chart shown in Fig. 14-1.

[Fig. 15-3] Fig. 15-3 represents a potential diagram corresponding to another certain timing of the timing chart shown in Fig. 14-1.

[Fig. 16-1] Fig. 16-1 represents a potential diagram corresponding to another certain timing of the timing chart shown in Fig. 14-1.

[Fig. 16-2] Fig. 16-2 represents a potential diagram corresponding to another certain timing of the timing chart shown in Fig. 14-1.

[Fig. 16-3] Fig. 16-3 represents a potential diagram corresponding to another certain timing of the timing chart shown in Fig. 14-1.

[Fig. 17] Fig. 17 is a view showing one example of a layout of approximately one pixel adopting a planar type storage capacitor element in the CMOS image sensor of the fifth embodiment according to the present invention.

[Fig. 18-1] Fig. 18-1 is a cross-sectional view showing a detail of a floating region area of a CMOS image sensor of a sixth embodiment according to the present invention.

[Fig. 18-2] Fig. 18-2 is a cross-sectional view showing a manufacturing step of the CMOS sensor shown in Fig. 18-1.

[Fig. 18-3] Fig. 18-3 is a cross-sectional view showing another manufacturing step of the CMOS sensor shown in Fig. 18-1.

[Fig. 19-1] Fig. 19-1 is a cross-sectional view showing a structure of a CMOS sensor of a seventh embodiment according to the present invention.

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[Fig. 19-2] Fig. 19-~~1~~2 is a cross-sectional view showing the structure of the CMOS sensor of the seventh embodiment according to the present invention.

[Fig. 20-1] Fig. 20-1 is a cross-sectional view showing the structure of